REMARKS

Claims 1, 7 and 13 have been amended.

Claims 1-18 are pending and under consideration. Reconsideration is respectfully requested.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 2, claims 1-18 are rejected under 35 U.S.C. § 103 in view of "OpenMP Fortran Application Program Interface," Version 1.1. November 1999 ("OpenMP") and U.S. Patent No. 5,151,991 to Iwasawa ("Iwasawa"). The rejection is traversed and reconsideration is requested.

On page 3 of the Office Action, it is correctly recognized that OpenMP fails to teach or suggest, "detecting a parallelization directive described by a user in said program source" as recited by amended claim 1. Further, OpenMP fails to teach or suggest "if said parallelization directive is detected, generating a front-end intermediate language," as recited in amended claim 1.

Further, the Applicants respectfully submit that Iwasawa fails to make up for the deficiencies of OpenMP. FIG. 3 and corresponding description in Iwasawa provides parsing 13 receiving a source program 11 of FORTRAN as its input and converts it to an intermediate language 6. Receiving this intermediate language 6 as the input, middle process 14 makes optimization and parallelization to modify the intermediate language 6. See FIG. 3 and column 5, lines 58-63. In FIG. 5, means for parallel processing is determined by filling each field from the outermost loop to inner loops in accordance with the loop tables shown in FIG. 5. See column 6, lines 11-19. First of all, a pointer is given to the loop table 22 in FIG. 5 corresponding to the leading loop DO 10, loop 16-21 on the outmost side in FIG. 4. Also, Iwasawa describes that the processing may be made sequentially from the outer loop. See column 6, lines 27-32.

Although Iwasawa does mention providing an intermediate language, filling each field in the table shown in FIG. 5 from the outermost loop, and processing sequentially, the description of Iwasawa fails to teach or suggest that the intermediate language is a front-end intermediate language as recited in claim 1. Further, Iwasawa fails to teach or suggest that the intermediate language is generated "by positioning on a storage region, each processing code of at least part of the parallelization directive with **a hierarchical structure in accordance with an internal**

structure of said parallelization directive," emphasis added, as recited in independent claim 1.

Instead, Iwasawa discloses a problem occurring when parallel processing is used in the program (see column 1, lines 22-23). Iwasawa further discloses that if instructions for parallelization are used, the instructions for parallelization must be changed whenever the characteristics of the hardware change (see column 1, lines 44-46). Thus, Iwasawa teaches away from using "parallelization directive" as disclosed in the claimed invention.

There is no teaching or suggestion in Iwasawa that the processing of the intermediate language is done by positioning each processing code in a hierarchical structure. Instead, Iwasawa limits its description to providing that the processing may be done sequentially. Rather than providing that each processing code of at least part of the parallelization directive positioned with a hierarchical structure, a dynamic number is determined of executed instructions per iteration of a loop in filed 27. See column 6, lines 34-62.

According to the American Heritage Dictionary, a copy of which is provided herein, sequential is defined as following of one thing after another; succession. See American Heritage Dictionary, Fourth Edition, page 1588. In contrast, hierarchical is defined as relating to hierarchy or a series in which each element is graded or ranked. See American Heritage Dictionary, Fourth Edition, page 826, hierarchy (definition #3).

FIG. 13 of Iwasawa provides a mode during the execution of an object code. However, FIG. 13 does not show that "each processing code of at least part of the parallelization directive with a hierarchical structure in accordance with an internal structure of said parallelization directive," as recited in independent claim 1. Rather, FIG. 13 of Iwasawa limits to illustrating processor 1 to processor NPE. But nothing in the cited reference teaches or suggest that a hierarchical arrangement is provided to position the processing code.

Thus, even assuming *arguendo* that OpenMP and Iwasawa were combined, a combination thereof would be silent in teaching or suggesting all of the features as recited in amended claim 1.

Although the above comments are specifically directed to claim 1, it is respectfully submitted that the comments would be helpful in understanding differences of various other rejected claims over the cited reference. Therefore, it is respectfully submitted that the rejection is overcome.

CONCLUSION:

In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore, defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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